

## *IEEE 1588 PTP Solutions*

- Protocol Software (V2) including TSU Support
- FPGA IP Core
- Services

# Every system or device can be synchronized with the IXXAT IEEE 1588 PTP Solutions.

## Introduction

IEEE 1588, also known as the "Precision Time Protocol" (PTP), defines a method to precisely synchronize the system clock of distributed nodes in a system using standardized packet based networks like Ethernet. The Precision Time Protocol allows all nodes to synchronize system-wide in the sub-microsecond range. In the past, such a synchronization performance was only possible by hard-wired synchronization busses or systems that implemented atomic clocks or GPS receivers on every node. With IEEE 1588, this can be achieved via standard communication busses and standard network interfaces.

Version 2 of the IEEE 1588 standard is a consistent improvement of version 1 to enhance the usability and precision for very large networks

and other applications, e.g. for the telecommunication market. To achieve these goals, V2 defines shorter synchronization frames to save network bandwidth, transparent clocks to avoid exponential error propagation in cascaded networks and many other new features. Additionally, the V2 standard introduces unicast connections to allow the synchronization of devices over long distance connections or via non-1588 devices (e.g. routers).

Version 2 is much more flexible regarding the configuration of the protocol by means of configuration sets used by specific devices. These sets, known as "profiles", simplify the configuration of the nodes and guarantee the proper behaviour and performance for specific systems.

## IEEE 1588 V2 Protocol Software

The IEEE 1588 V2 protocol software enables simple and rapid development of IEEE 1588 compliant devices. The IEEE 1588 protocol software developed by IXXAT has a modular structure to ensure fast integration into the target system. To access the UDP/IP socket, the target platform interfaces are composed in a separate adaptation layer (network interface), that considerably simplify porting to the target system.

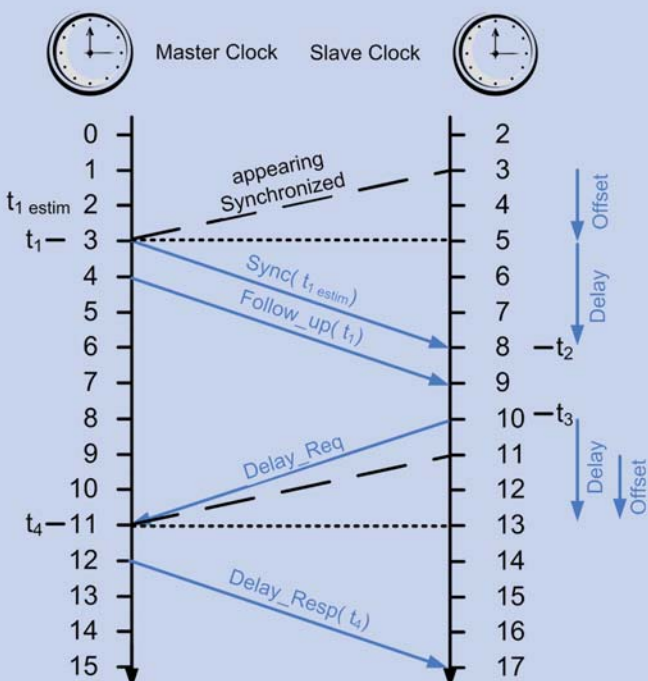
The software is completely independent of the operating system and therefore, can also be used in applications without an operating system (i.e. superloops). The only requirement is an UDP/IP stack supporting multicasts. The IEEE 1588 stack is highly scalable and can be ported to almost any device. It supports message intervals for up to 2048 packets per second for each message type.

### Features

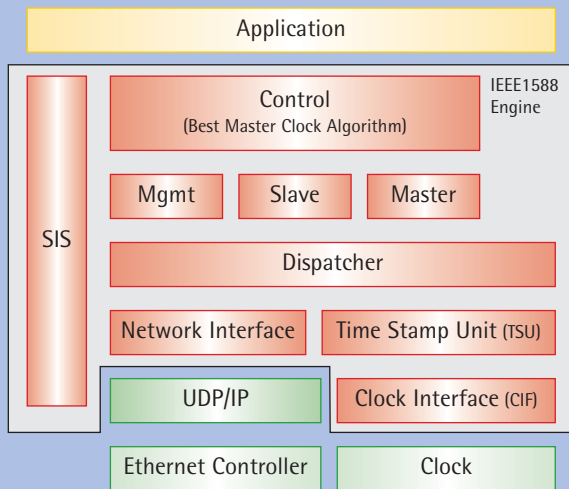
The IEEE 1588 V2 software is a full implementation of the standard, including some additional features:

- Ordinary and Boundary Clock
- Transparent Clock
- Unicast Messaging
- Best Master algorithm
- One step and two step support

IEEE 1588 Synchronization Cycle



Structure of the IEEE 1588 Protocol Software



- Management Protocol / Interface
- Simple API for interfacing to the application
- Works with or without OS
- Easily portable to target hardware, UDP/IP stack and OS
- Support of integrated Hardware Time Stamping Units (TSUs)

Delivery Contents

- "C" Source code
- Freescale PowerQUICC MPC8360 reference implementation
- Demo implementation for PCs running Microsoft Windows
- Software license
- User Manual

Evaluation Versions

Evaluation versions are available for the Freescale MPC 8313/8360 development systems and COMExpress boards and for the AMCC PPC405EZ Acadia Board including TSU support. The evaluation versions can be downloaded from the IXXAT web site.

# IEEE 1588 IP Core Module for FPGAs

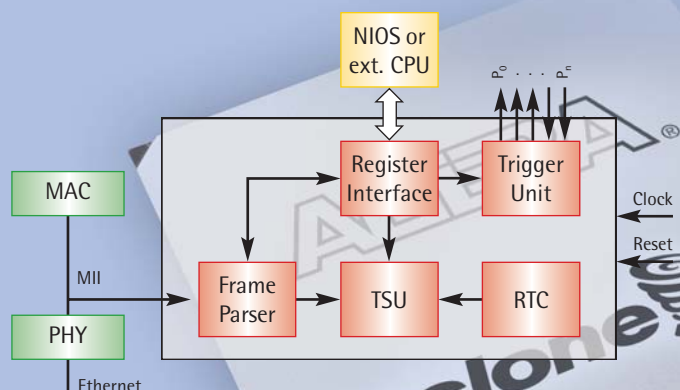
For the clock synchronization of the local real-time clock with the master clock, it is necessary to provide very accurate time stamps for the IEEE 1588 telegrams. If the CPU in use does not support IEEE 1588 in

hardware, it is necessary either to use software time stamping or to use an external IEEE 1588 real time clock (RTC) with a time stamping unit (TSU). If the time stamp is generated by software, the clock synchronization is in the range of several 10 μs up to milliseconds.

If implemented in hardware (FPGA), the accuracy for the time stamp generation corresponds to the FPGA internal clock, which is in the range of 20 to 50 ns. The synchronization of master clock and slave clock in the sub-microsecond range is possible.

The generation of trigger signals on selected output ports can be implemented by using additional logic provided by the IP Core. Frequency and offset are programmable by an assigned timer unit. The generation of time stamps based on signal pulses and rising or falling edges on the input ports is also possible.

Structure of the IEEE 1588 IP Core



The IEEE 1588 IP Core provides two different solutions:

- Execution of the IEEE 1588 protocol software on the FPGA internal soft CPU, e.g. the Altera NIOS (IEEE 1588 device as one chip solution).
- Usage of an external CPU to execute the IEEE 1588 protocol software and application software.

For both solutions there are no special real-time requirements for the software environment. It is absolutely sufficient to execute the IEEE 1588 protocol software cyclically, approximately every 10 to 100 ms. This leads to a CPU load of less than 1% to perform the IEEE 1588 functionality.

## Features

- Real time clock setting and alignment via software.
- Generation of time stamps by external input signals via the trigger unit.
- Control of external output signals based on configurable timers.
- MII interface for incoming and outgoing sync message detection.
- Support of IEEE 1588 version 1 and 2.
- Standard address/data bus interface to allow the adaptation to various CPU interfaces.
- Message buffer for message headers and time stamps for the correct correlation of the TCP/IP packets by the protocol software.
- Variable external clock frequencies possible.
- Generation of an external PPS signal for accuracy measurements.

## Delivery Contents

- 1588 MegaCore function for Altera FPGAs
- User manual
- Quick start guide

## Technical Data

The IEEE 1588 IP Core needs about 2000 logic elements on an Altera FPGA. With an external 50 MHz clock the accuracy is better than  $\pm 150$  ns.

The IEEE 1588 IP Core can be ported to Lattice and Xilinx FPGAs on customer request.

## Services

### Maintenance

IXXAT offers maintenance for the software package including free updates and technical support during the maintenance period.

### Implementation support

IXXAT adapts, implements and tests the IEEE 1588 V2 Protocol Software and the IEEE 1588 IP Core on your hardware or in your application.

### Training

To provide a quick start with IEEE 1588 IXXAT offers a two day in-depth technical training course conducted by experienced instructors.

The seminar is targeted both at system integrators or device developers in charge of IEEE 1588 implementations and decision makers that need the background information required to assess the technology.

The training course is held in German language at a regular schedule at the IXXAT main offices in Weingarten (Germany) or on request as in-house seminar in German or English language.