

A Universal Approach for implementing Real-Time Industrial Ethernet



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1 Introduction

“Industrial Ethernet” is a broad term that generally refers to two distinct types of networking: (1) non- or Soft-Real-Time (SRT), which is primarily characterized by information processing and (2) Isochronous Real-Time (IRT), which offers deterministic control messaging for high performance factory floor equipment.

An example of SRT would be a warehouse in which the enterprise network has to communicate information to and from a barcode scanner in the receiving department. In this example, seconds or even minutes are perfectly acceptable update rates for this level of processing.

In a production environment, there may be a machine for which IRT characteristics must be employed. In such machines, it is necessary that the various sensors and actuators communicate very fast and with determinism. Fieldbus communication such as Profibus, DeviceNet, and CANopen are typically employed to transfer control data within milliseconds among the distributed sensors and actuators on a machine.

In order to improve machine throughput beyond the fieldbus data rates, Ethernet is considered to be a faster messaging transport layer.

Ethernet, by itself, is inherently non-deterministic and cannot guarantee that all nodes on a network will be able to access the network within a specified time, a requirement in IRT applications. To circumvent this deficiency, measures have been taken, by virtue of the many Industrial Ethernet standards, to insure that all nodes on a network are able to transmit data within less than a millisecond. Slower performance (i.e. greater than a millisecond cycle time) does not justify the additional expense of using a higher-cost 32-bit Ethernet device over an 8 or 16-bit lower-cost fieldbus device for IRT-type communication.

An exception to this may be the number of nodes required. Fieldbus systems have node limitations. Ethernet can handle many more nodes than a fieldbus and in the same amount of time. For example, a CAN bus with 3 to 7 nodes can achieve a cycle time” of 2 to 4 ms whereas an Ethernet network with 30 to 100 nodes can achieve the same update rates.

2 IRT Industrial Ethernet Performance Criteria

Two important criteria associated with IRT Ethernet that affect performance are:

1. Minimum cycle time.
2. Number of devices on the bus which can be updated during one cycle period.

Cycle Time

Most IRT Ethernet applications target a cycle time of 500 μ s. In some applications, 200 μ s are required, but there are generally less nodes. The cycle time is determined by the total of all communications on the bus. Since every individual node performs specific tasks, there are also node-internal processes like Network Management and Cycle State Machine tasks that must be considered. When considering an IRT Ethernet standard, it is important to calculate cycle times that take into account all the message events on the bus.

Number of Devices

In combination with the cycle time, the machine builder or system integrator will be most interested in the number of devices which can be deployed on one Ethernet bus while maintaining the required minimum cycle time, the latter being a requirement generated by the production process. The higher the number of devices on a single bus, the more cost efficient the overall system will be since infrastructure components like Gateways can be minimized.

In order to optimize these factors, the architects of the IRT Ethernet standards prescribe a portion of hardware state machine data processing in every node. This guarantees the low level communication part of each node to be 100% deterministic with respect to message processing and a predictable order of the packets during a communication cycle.

Since this extra hardware state machine based processing capability cannot be typically found on microcontrollers today, it becomes necessary to add either specific ASICs or an FPGA into the automation device.

3 Industrial Ethernet Standards

At last count, there were nineteen Industrial Ethernet protocols announced by various vendors. However, only six of these are generally regarded as open standards. EtherNet/IP, Profinet IO, and MODbus TCP are popular SRT choices. ETHERNET Powerlink (EPL), SERCOS III, EtherCAT, and Profinet IRT are being deployed in IRT applications such as motion control.

Protocol	Real-time	FPGA	Typical Cycle Times
Ethernet/IP	SRT	Standard MAC + Protocol Stack on NIOS	> 10 ms
ProfiNet IO	SRT	Standard MAC + Protocol Stack on NIOS	> 10 ms
Modbus/TCP	SRT	Standard MAC + Protocol Stack on NIOS	> 10 ms
ETHERNET Powerlink	IRT	Standard MAC with specific packet handling Protocol Stack on NIOS	< 500 μ s
SERCOS III	IRT	Bus Specific IP	31.5 μ s
EtherCAT	IRT	Bus Specific IP	< 50 μ s
Profinet IRT	IRT	Standard MAC + Protocol stack on NIOS	< 1ms

The implementation strategies outlined in this article illustrate how an FPGA vendor and a protocol supplier have worked together to offer a single FPGA platform for the open SRT and IRT protocols listed in this article. With this comprehensive and flexible solution, FPGAs enable equipment vendors to design a single hardware platform that can be installed with application-relevant SRT and IRT protocols. This process avoids costly development time and vastly increases the communication flexibility of the OEM's and supplier's products without affecting the application process.

4 FPGA Architecture Provides a Flexible Mix

Today's state-of-the art FPGAs are more than just a programmable resource providing a certain number logical cells. The loadable soft cores enable the user to create a scaleable microcontroller within an FPGA and equip it with ultra fast peripherals like Ethernet Controllers, DRAM Controllers or UARTs on the same silicon.

Industrial Ethernet users especially benefit from this architecture because of the specific, and sometimes proprietary, mechanisms required by IRT Ethernet standards which cannot be found on the usual microcontroller platforms. Furthermore, an FPGA offers several different connection interfaces to microcontrollers such as memory mapping or SPI.

4.1 SRT Protocols on an FPGA

ProfiNet IO "Device" and EtherNet/IP "Adapter" protocols can be fully executed on the Nios II embedded processor of the FPGA, both stacks make use of a standard TCP/UDP/IP stack without specific real time requirements. However, due to performance optimization, the cyclic I/O data are communicated directly with the Ethernet Controller bypassing the Profinet or Ethernet/IP stack (left path) while configuration or service data must go through the stack. Additionally the FPGA implementation of ProfiNet and Ethernet/IP provides a direct TCP/IP communication path which can be used for general purpose protocols such as http or ftp.

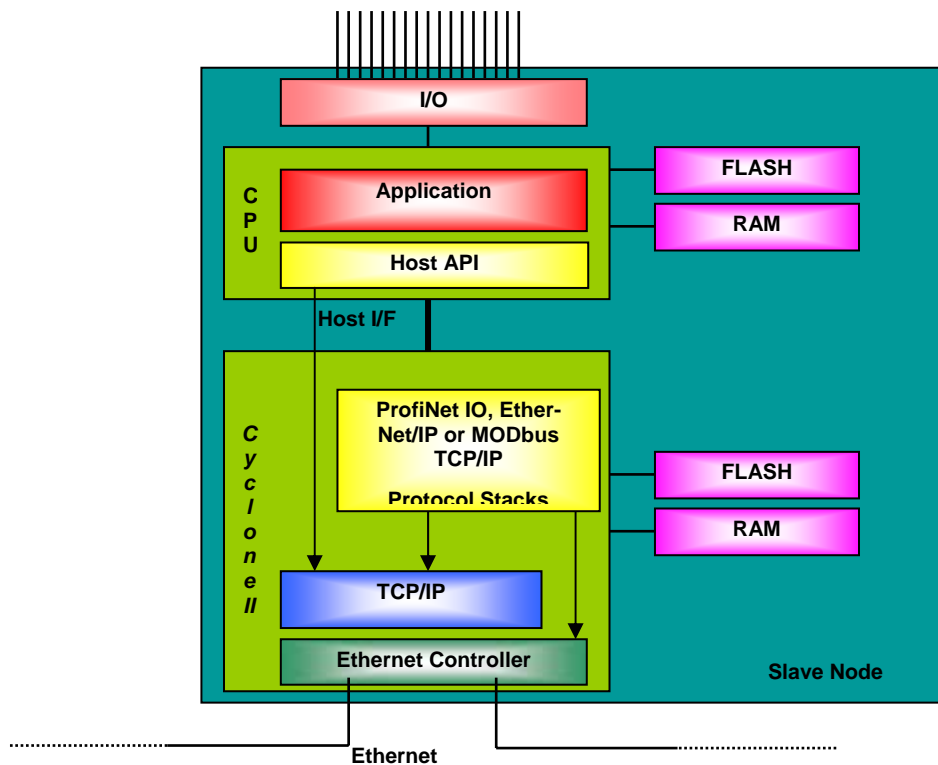


Figure 1: SRT Protocols Implemented on an FPG

4.2 IRT Protocols on an FPGA

4.2.1 ETHERNET Powerlink

The implementation of a Powerlink Controlled Node (Slave) on an FPGA provides a very powerful and highly flexible solution. The FPGA contains an Ethernet Hub and an Ethernet Controller/EPL packet handler. In addition, a 32-bit CPU core is also included in the FPGA. This processor core provides the flexibility to execute a scalable amount of software. For slower I/O, the whole EPL stack plus I/O application software can be implemented without a Host CPU. For faster Controlled Nodes, only the EPL stack has to be implemented. The most important advantage of this approach is that the Host CPU is isolated from the ETHERNET Powerlink's critical real-time processes.

Figure 2 illustrates the Host CPU with additional FPGA containing the CPU core. The application code is executed on the Host CPU and the EPL Stack is executed on the FPGA.

This achieves shorter cycle times down to 250µs. Additionally, the FPGA contains an optimized Ethernet Controller with a hardware IP filter as well as a fast response mechanism and Hub, which guarantees ultra low response times of less than 1 µs. Hub latency is approximately 400 ns.

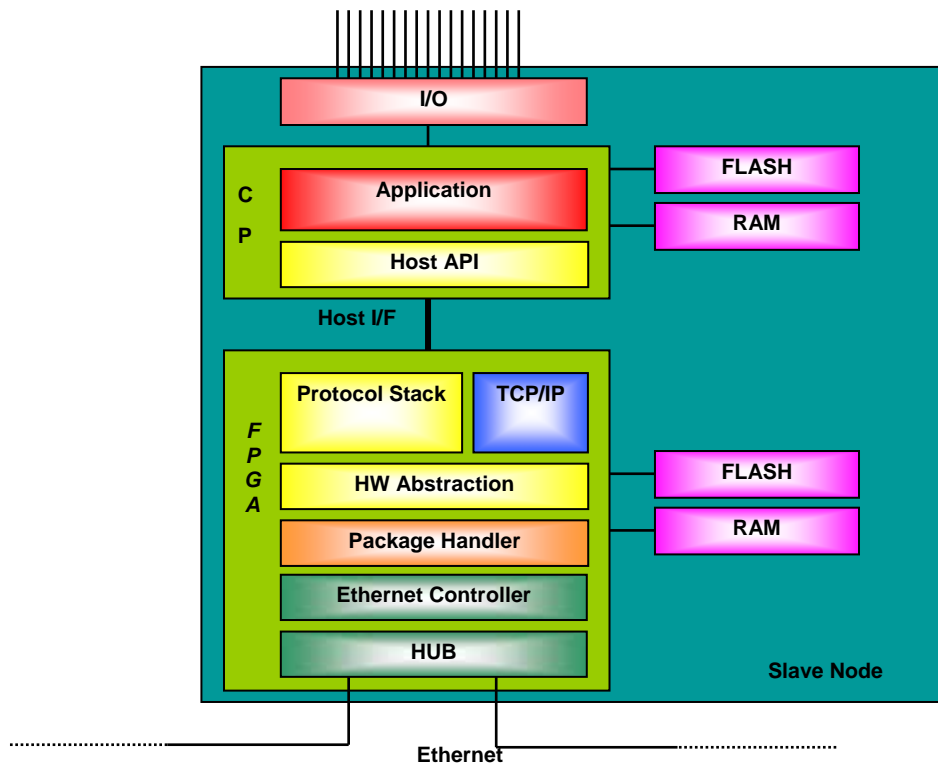


Figure 2: ETHERNET Powerlink with an FPGA as a Communication Processor

4.2.2 SERCOS III and EtherCAT

SERCOS III and EtherCAT are the two IRT protocols meeting highest real time requirements. To achieve this performance, specific Ethernet MACs are required. These Specific Ethernet MACs are available as routable net lists and have been implemented in the FPGA by providing the necessary number of logic cells. Figure 3 illustrates how EtherCAT is implemented on an FPGA while the CPU executes the “CANopen over EtherCAT” CoE protocol software and the application is executed on the Host CPU.

The EtherCAT protocol can be scaled to the extent necessary for different device types. Typical consumption of logical cell for a synchronized servo drive is 12-15 kcells.

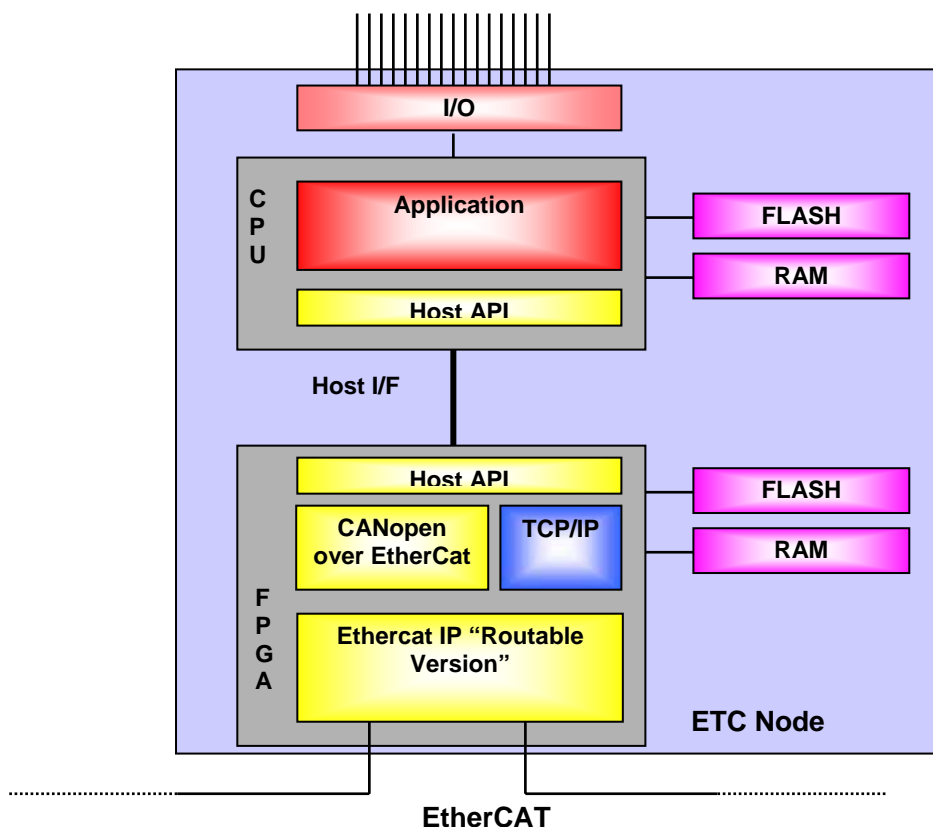


Figure 3: EtherCAT Implementation on an FPGA

5 Conclusion

For industrial automation equipment vendors and users, interoperability is no longer a barrier when deploying the solutions presented in this article. Of profound importance is the ability for sensor and actuator vendors to employ one FPGA device that supports multiple Industrial Ethernet protocols. The ability of a CPU-enabled FPGA operating as a communication processor in conjunction with an application processor offers very tangible advantages in terms of reducing up-front development costs as well as increasing performance of such a solution.